



Banana Pi Compute Module 4

A Banana Pi for deeply embedded application

Colophon

法律信息及版权信息

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Chapter 1. Introduction

1.1 Introduction

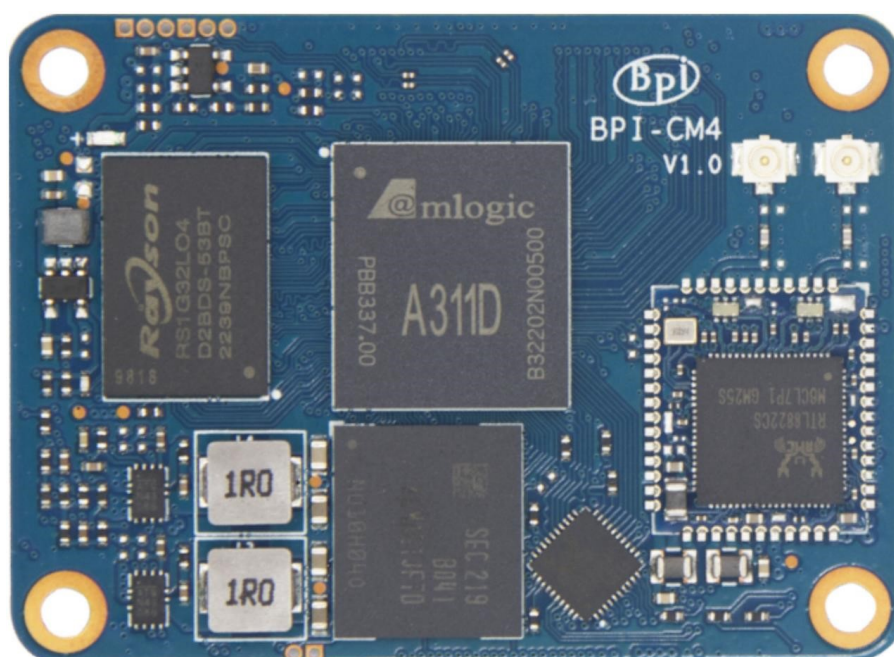


Figure 1. The BPI-CM4

The Banana Pi Compute Module 4(CM4) is a System on Module(SoM) containing processor, DRAM, eMMC Flash and supporting power circuitry. These modules allow a designer to use the Banana Pi hardware and software stack in their own custom systems and form factors. And, These modules offer additional IO interfaces beyond what is provided on Banana Pi boards, providing designers with more options.

The design of the CM4 is loosely based on the Amlogic A311D, Quad core ARM Cortex-A73 and dual core ARM Cortex-A53 CPU, ARM G52MP4(6EE) GPU, NPU for AI at 5.0 TOPS, support Camera and MIPI-CSI interface, HDMI output, 2 Gigabit port, 4G RAM and 16 GB eMMC flash.

for A311D chip PIN limited. just support 1 HDMI, 1 CSI and 1 DSI, Raspberry Pi support 2 HDMI, 2 CSI and 2 DSI, Other is Pin2Pin. you can use Raspberry Pi CM4 baseboard.



for A311D chip PIN limited. just support 1 HDMI, 1 CSI and 1 DSI, Raspberry Pi support 2 HDMI, 2 CSI and 2 DSI, Other is Pin2Pin. you can use Raspberry Pi CM4 baseboard.

1.2 Key Feature

Key feature of the BPI-CM4 are as follows:

- Amlogic A311D Quad core ARM Cortex-A73 and dual core ARM Cortex-A53,ARM G52 MP4(6EE) GPU
- NPU for AI Next generation, deep-neural-network applications, at 5.0 TOPS
- OpenGL ES 3.2, Vulkan 1.1 and OpenCL 2.0 support
- 4GB LPDDR4 RAM
- 16GB eMMC flash (Max 128G)
- MIPI DSI :
 - 1x4-Lane MIPI DSI Display Interface
- MIPI CSI :
 - 1x4-Lane MIPI CSI Camera Interface
- PCIe Interface:
 - 1xPCIe 1-Lane Host,Gen 2(5Gbps)
- HDMI Interface:
 - 1xHDMI 2.1 Output Interface(up tp 4Kx2K@60)
- Gigabit Ethernet PHY supporting
- 26 PIN GPIO:
 - 1x PCM
 - 1x IIC
 - 1x UART
 - 1x PWM
- Single +5V PSU Input
- Support Android and Linux system
- Size: 55x40mm

Chapter 2. Interfaces

2.1 Wireless

The BPI-CM4 supports an onboard wireless module based on Realtek RTL8822CS, supports both

- 2.4GHz & 5GHz IEEE 802.11 a/b/g/n/ac 2x2 MIMO wireless
- Bluetooth 5.0 BR/EDR/LE

These wireless interfaces can be individually enabled or disabled as required via CPU GPIO. In the case of many application environments, a service engineer can enable wireless operation and then disable it when done.

The CPU can also turn on the wireless by itself for data communication, and turn off the wireless after completion to reduce power consumption.

The BPI-CM4 has two standard IPEX-1G connector on the module, If you want to use 2x2 MIMO, need to connect 2x 2.4G&5G antenna.

Banana Pi Ltd has an antenna kit which is certified to be used with the BPI-CM4. If a different antenna is used then separate certification will be required.

2.2 Ethernet

The BPI-CM4 has an onboard Gigabit Ethernet PHY - the [REALTEK RTL8211F](#) - some of the major features of this PHY include;

- IEEE 802.3az-2010
- Built-in Wake-on-LAN
- Crossover Detection & Auto-Correction

A standard RJ45 connector is necessary to provide an Ethernet connection to the BPI-CM4. Can be seen in [Figure 2](#)

[EthSch] | *EthernetSch.jpg*

Figure 2. Ethernet Schematic

The differential Ethernet signals should be routed as 100Ω differential pairs, with suitable clearances. Length matching between pairs should be better than 50mm, so in the typical case no length matching is required. However the signals within a pair need to be length matched, ideally to better than 0.15mm.

The PHY also supports up to 2 LEDs to give user status feedback, these are low active. These LEDs can have a range of functions, and you should consult your OS driver to see

which functions are supported by your driver.

2.3 PCIe(Gen2 x1)

The BPI-CM4 has an internal PCIe2.0 x1 host controller. Connecting a PCIe device follows the standard PCIe convention. The CM4 has onboard AC coupling capacitors for **PCIe_CLK** and **PCIe_TX** signals. However the **PCIe_RX** signals need external coupling capacitors close to the driving source (the device **TX**), if you are using an external PCIe/NVMe cards these capacitors will be onboard. The PCIe conversion is that if you are wiring directly to an IC then the TX and RX pairs need to be swapped (TX → RX, RX → TX). If you are wiring to a connector then this is typically labelled from the host post of view and so TX RX swaps aren't required. Additionally the **PCIECK_REQN** must be connected to ensure the CM4 produces a clock signal, and the **PERST0_N** should also be connected to ensure the device is correctly reset when required. The differential PCIe signals should be routed as 100Ω differential pairs, with suitable clearances. There is no need to match the lengths between pairs, only the signals within a Pair need to be length matched ideally to better than 0.1mm



5.10 kernel and

2.4 USB 2.0(HS)/3.0(SS)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Ω differential pair. The P N signals should ideally be matched to better than 0.15mm.



USB 3.0 or PCIe 2.0 x1

USB 3.0 multiplexed with **PCIe 2.0 x1**. **USB30_RX_P/N** multiplexed with **PCIe_RX_P/N** and **USB30_TX_P/N** multiplexed with **PCIe_TX_P/N**.

BPI-CM4 has two full-speed USB channels, one of which (USB_A) can be USB2.0 x1+ PCIe2.0 x1 or USB3.0 x1, or can use FE1.1s chip (USB 2.0 HUB chip) or VL807 (USB 3.0 HUB chip) Expanded to four-way USB. The other one (USB_B) interface also has OTG(On-The-Go) function at the same time.

2.5 GPIO

BPI-CM4 has 17 pins available for general purpose I/O (GPIO), corresponding to the first half of the standard 40 pins of other BananaPi development boards. These pins have access to internal peripherals; PCM, IIC, UART and PWM. [BPI-CM4 Sch](#) describes these features in detail, and the multiplexing options available. The drive strength and slew rate should ideally be set as low as possible to reduce any EMC issues. GPIOX_17 and GPIOX_18 have 2.2K pull up resistors.

By default, GPIO bank is powered by 3V3, but GPIOX_x GPIOs can be changed to powered by 1.8V.



GPIOX_x Power Bank depending on the selected WiFi module, PCIe WiFi or RTL WiFi (default) is powered by 3.3V, and AMPAK 6275s WiFi is powered by 1.8V.

[GPIO] | *GPIO.jpg*

Figure 3. GPIO

2.5.1 Alternative Function Assignments

Table 1. GPIO Alternative Function Assignments

Num	GPIOx_x	PD/PU	ALT0	ALT1	ALT2
3	GPIOX_17	PU	GPIO	I2C_EE_M2_SDA	BT_EN
5	GPIOX_18	PU	GPIO	I2C_EE_M2_SCL	BT_WAKE_HOST
7	GPIOH_5	PU	GPIO	SPDIF_IN	
8	GPIOX_6	PU	GPIO	UART_B_TX	WIFI_PWREN
10	GPIOx_7	PU	GPIO	UART_B_RX	WIFI_WAKE_HOST
11	GPIOAO_10	PD	GPIO		
12	GPIOA_1	PU	GPIO	I2SB_SCLK	
13	GPIOH_4	PD	GPIO	SPDIF_OUT	
15	GPIOAO_5	PU	GPIO	IR_IN	
16	GPIOA_0	PU	GPIO	I2S_MCLK	
18	GPIOA_2	PD	GPIO	I2SB_LRCLK	
19	GPIOX_8	PU	GPIO	SPI_A_MOSI	BTPCM_DIN
21	GPIOX_9	PU	GPIO	SPI_A_MISO	BTPCM_DOUT
22	GPIOA_7	PU	GPIO	I2SC_DOUT_DIN_3	
23	GPIOX_11	PU	GPIO	SPI_A_CLK	BTPCM_CLK
24	GPIOX_10	PU	GPIO	SPI_A_SS0	BTPCM_SYNC
26	GPIOA_3	PU	GPIO	I2SB_DOUT_DIN_0	

2.6 HDMI

The BPI-CM4 supports one HDMI 2.1 interface, it capable of driving 4Kx2K 60fps output.

HDMI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm. Pairs don't typically need any extra matching as

they only have to be matched to 25mm.

CEC, Dynamic HDR and HDCP 2.2 supported. CEC internal 27K pullup resistor and **HDMI_SDA/HDMI_SCL** internal 27K pullup resistor is included in the BPI-CM4.

The BPI-CM4 need extra ESD protection maybe required.

2.7 CSI(MIPI Serial Camera)

The BPI-CM4 supports one camera ports(4 lanes); CSI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm.

The documentation around the CSI interface can be found on the [BananaPi Wiki](#) website while Linux kernel drivers can be found on [Github](#).



Camera sensors supported by the official BananaPi firmware are;ShenZhenShi HongJia OS08A10 V11(sensor: OS08A20). no security device is required on Compute Module devices to use these camera sensors.

2.8 DSI(MIPI Serial Display)

The BPI-CM4 supports one display ports(4 lanes); supports a maximum of data rate per lane of 1Gbit/s.

The DSI interface only supported by offical BananaPi firmware are supported DSI Displays, more infomation can see [BananaPi Wiki](#) website.DSI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm.



BananaPi firmware only supports officially recommended DSI displays, but add and compile your own driver.

2.9 IIC(GPIO Pin3&Pin5)

This IIC bus is not shared with CSI or DSI and can be used arbitrarily.

2.10 IIC(CAM0_SCK/SDA)

This IIC bus(GPIOH_7/GPIOH_6) is used by default for MIPI CSI(Camera sensor), If you don't use, it can also be used for general purpose I/O or to connect other IIC devices.

2.11 IIC(TP_SCK/SDA)

This IIC bus(GPIOA_15/GPIOA_14) is used by default for MIPI DSI Touch Panel(capacitive touch panel), If you don't use, it can also be used for general purpose I/O or to connect other IIC devices.



All IIC buses have 2K2 pull-up resistors on BPI-CM4

2.12 SDIO/eMMC()

The BPI-CM4 supported 16GB eMMC flash (option up to 128GB). The **TF_VDD_EN** signal is used to enable an external power switch to turn on power to the TF_Card. If booting from TF_Card is required then a pullup resistor must also be fitted to default the power to be on.

[TF_CARD] | *TF_Card.jpg*

Figure 4. TF Card

2.13 Analog(SARADC_CH2/CH3)

These are the two ADC pins straight out of the CPU.No onboard filtering, 100K pull-up resistors on BPI-CM4.



If you need to use these two ADC pins, you need to consider adding filtering, the recommended value is 1000pF ~ 0.1uF

2.14 CPU_RST

Pulling this pin low places BPI-CM4 in reset. Removing the pull-down state allows the BPI-CM4 to reset and run again.



To reset BPI-CM4, the **CPU_RST** pin needs to be pulled low for at least 0ms. $T_{CPU_RST_L} > 0ms$.

2.15 SYS_LED

This pin is designed to drive an LED to show the BPI-CM4 operating status. If an error occurs during startup, it will blink with the **SYS_LED2** beyond expectations to help the user easily determine the status.

2.16 SYS_LED2

This pin is designed to drive an LED to show the BPI-CM4 operating status. If an error occurs during startup, it will blink with the **SYS_LED2** beyond expectations to help the user easily determine the status.

Chapter 3. Electrical and Mechanical

3.1 Mechanical

The BPI-CM4 is a compact $40 \times 55\text{mm}$ module. The Module is 4.1mm deep, but usually the height after connection is 4.4mm.



The height of 4.4mm after connection is the minimum height between the connector and the fixing stud recommended by bpi. If other connectors and fixing studs of the corresponding height are used, the height needs to be actually measured.

1. $4 \times \text{M3}$ Mounting holes (inset about 4mm from module edge)
2. PCB thickness $1.2\text{mm} \pm 10\%$
3. [Amlogic A311D](#) SoC height including solder balls $1.0 \pm 0.11\text{mm}$
4. Stacking height either:
 - a. 1.5mm with mating connector (clearance under CM4 0mm) : DF40C-100DS-0.4v
 - b. 3.0mm with mating connector (clearance under CM4 1.5mm): DF40HC(3.0)-100DS-0.4v

If the wireless antenna is used it must be orientated towards the edge of the plastic enclosure and any close by metal must have cut outs or the wireless performance will be degraded. It is recommended to fix the antenna outside the case.

[Mechanical] | *Mechanical.jpg*

Figure 5. Mechanical



The location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however the maximum component heights and PCB thickness will be kept as specified.

3.2 Thermal

The BPI-CM4 has less passive cooling due to its smaller size, so it may run hotter. In order to ensure the life of BPI-CM4, the core temperature of the main control chip (Amlogic A311D) should be kept below 85 degrees Celsius as much as possible. If the core temperature is found to be higher than 85 degrees Celsius, you can reduce the clock frequency or add additional active and passive cooling methods.

It is important that thermal solution chosen keeps the ambient temperature for the other silicon devices on the CM4 within the operating temperature range.

Operating temperature range: -20°C - +85°C Non-condensing.

3.3 Electrical Specification



Stresses above those listed in Table 3 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	+5V_Input	-0.5	6	V
V _{GPIO_ref}	GPIO Voltage	-0.5	3.6	V
V _{GPIO}	GPIO INPUT Voltage	-0.5	V _{GPIO_ref} +0.5	V

DC Electrical Characteristics

Table 3. Normal GPIO Specifications (For DIO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH(gpio)}	High-level Input Voltage	IOVREF/2+0.3		VDDIO+0.3	V
V _{IL(gpio)}	Low-level Input Voltage	-0.3		IOVREF/2-0.3	V
R _{PU/PD}	Built-in pull Up/Down resistor		60K		ohm
IoH/IoL	GPIO driving capability	4 ¹⁾		6 ²⁾	mA
VOH	Output high level with 4 mA loading	VDDIO-0.5			V
VOL	Output low level with 4 mA loading			0.4	V



Minimal driving capability applies when VDDIO LV 1.71V, or VDDIO HV 3.0V, VOL<0.4V Maximal driving capability only applies to applications such as driving LED when VOL<0.6V.

Table 4. Open Drain GPIO Specifications (For DIO_OD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH(OD5V)}	High-level Input Voltage	2.2		5.5	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IL(OD5V)}$	Low-level Input Voltage	-0.3		0.8	V
$V_{IH(OD3.3V)}$	High-level Input Voltage	2.2		3.6	V
$V_{IL(OD3.3V)}$	Low-level Input Voltage	-0.3		0.8	V
$R_{PU/PD}$	No built-in pull up/down resistor on OD IO	-	-	-	ohm
I_o	OD IO driving low capability	4 ¹⁾		6 ²⁾	mA
VOL	Output low level with mini I_o loading			0.4	V



Minimal driving capability applies when VDDIO LV 1.71V, or VDDIO HV 3.0V, VOL<0.4V Maximal driving capability only applies to applications such as driving LED when VOL<0.6V.

Chapter 4. Pin Out

Table 5. Pin out define of BPI-CM4

||
||
||

Build

This page was built by the following command:

```
$ mvn
```

Attributes

Built-in

asciidoctor-version

2.0.20

safe-mode-name

unsafe

docdir

/home/qubot/CM4-Doc/src/docs/asciidoc

docfile

/home/qubot/CM4-Doc/src/docs/asciidoc/example-manual.adoc

imagesdir

images

Custom

sourcedir

/home/qubot/CM4-Doc/src/main/java

Includes



Includes can be tricky!